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A HIGH OUTPUT IMPEDANCE CURRENT SOURCE FOR WIDEBAND BIOIMPEDANCE SPECTROSCOPY USING 0.35µM TSMC CMOS TECHNOLOGY

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Abstract – In this paper, a wideband current source is presented. The current source is based from a Second Generation Current Conveyor (CCII) coupled to a Folded Cascade Operational Trans-conductance Amplifier (FC-OTA). The FC-OTA is configured as an inverting amplifier whose feedback loop acts as a current source. When driven by an input voltage source, this amplifier behaves as a Voltage-Controlled Current Source (VCCS). Instead of driving the VCCS by a voltage source, a Norton current source has been utilized in the form of a CCII. This effectively increases the output impedance of the current source especially at the higher frequencies. Such is a stringent requirement for an excitation current in a bio-impedance instrument. HSPICE simulations confirm the improvement of the output impedance at frequencies in the upper range of the beta dispersion frequency (10MHz) as compared to a voltage source drive. The current source has been designed using TSMC 0.35µm CMOS 2P4M Technology and dissipates only 600µW of power.

Keywords— Wideband Current Source, Output Impedance, Bioimpedance, Second Generation Current Conveyor, Folded-Cascode Operational Transconductance Amplifier

I. INTRODUCTION

Wide-band electrical bio-impedance spectroscopy is one of the developing technologies for the monitoring and analysis of tissue state and organ functions. This technology considers the electrical properties of biological tissues modelled as a network of resistors and capacitors or constant phase elements. The response of any biological tissue to an excitation current has been categorized into three dispersions namely: *alpha* (10Hz – 10kHz), *beta* (10kHz – 10MHz) and *gamma* (10MHz – 1GHz) [1]. The alpha and beta dispersion frequency ranges have been mostly applied in the clinical setting. These involve preliminary studies on the detection of hypertension and hyper-hydration of hemo-dialysis patients [2], pressure ulcer [3], and skin cancer [4].

In a typical bio-impedance instrument the sample is injected a high frequency current of amplitude in the range of micro- to milli-amperes. A high CMRR and high input impedance instrumentation amplifier is used to detect the voltage developed across the sample in either the two point or four point probe setup. The current source is normally driven by a voltage source forming a VCCS. The driving voltage source along with the detected bio-modulated voltage are used to obtain the impedance magnitude and phase information of the sample using synchronous demodulation or more commonly the lock-in approach.

One cause of measurement error in bio-impedance instruments is the finite output impedance of the current source. It is essential that high output impedance is maintained over the operating frequency range so that the injected current is constant and that the current source does not load the sample.

There have been several techniques to improve on the output impedance of a current source. Some utilize the Negative Impedance Converter

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(NIC) which creates an inductance to counter the effect of the capacitance at high frequencies. This however is delimited to single frequency applications as the effective inductance needs to be tuned to the capacitance. Other circuit topologies include Howland Current Sources [5], Current Conveyors [6] and Floating Mirrored Trans-conductance Amplifiers [7]. In this paper, a different approach is presented. A CCII that serves as a Norton current source drives an inverting amplifier VCCS. This has been done to increase the output impedance of the VCCS particularly in the higher end of the beta dispersion range. This is based from the concept presented in [8].

II. MEHODOLOGY

2.1. Current Source Implementation

Figure 1 shows the functional block diagram of the designed current source. As can be seen, the CCII drives the VCCS.

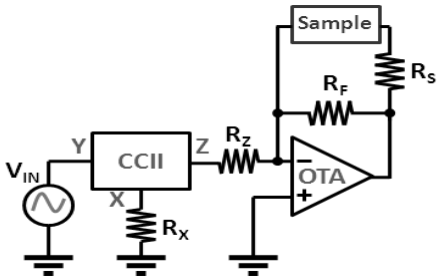


Figure 1. Proposed current source implementation

The output impedance of the CCII measured at its Z-terminal adds to the overall output impedance Z_{OCS} of the resulting current source. This is shown in Equation 1.

$$Z_{OCS} = R_S + R_F \| \left(Z_{OA} + R_{IN} \| Z_{IA} \right)(A_D + 1)\left(1 - \frac{1}{2CMRR}\right) \quad (1)$$

where:
Z_{OA} = output impedance of the OTA,
Z_{IA} = input impedance of the OTA,
A_D = differential gain of the OTA,
CMRR = OTA's common-mode rejection ratio
R_{IN} = output impedance of the CCII, and
R_S = series resistance to the sample.

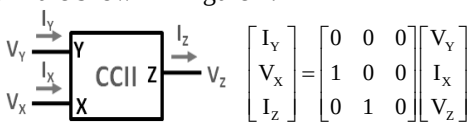
The value of R_{IN} is equal to:

$$R_{IN} = R_Z + Z_{OCC} \quad (2)$$

Based from (1) and (2), Z_{OCS} is directly proportional to the output impedance of the CCII (Z_{OCC}).

2.2. Second Generation Current Conveyor

The CCII's functional block and operational matrix are shown in Figure 2.



(a) (b)

Figure 2. (a) CCII Block and (b) Operational Matrix

The CCII consists of a voltage follower between the Y and X terminals and a unity gain current amplifier between the X and Z terminals. A current drained in the X-terminal is conveyed to the Z-terminal. The CMOS implementation of a CCII is shown in figure 3 [9].

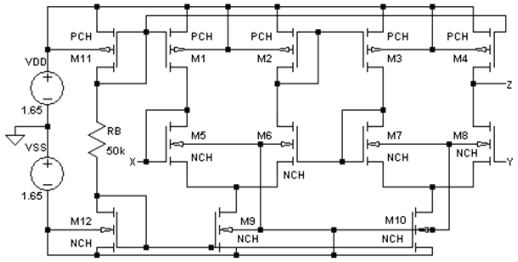


Figure 3. CMOS Implementation of the CCII [9]

The First Generation Current Conveyer (CCI) formed by M_2, M_3, M_6 and M_7 conveys the same voltage between the sources of M_6 and M_7, and the same current through M_2 and M_3. An input voltage at Y does not affect the current flowing through M_7 because it already follows the current at M6 via CCI action. Since the sources of M_5 and M_8 are held at the same voltage by the CCI and carries the same current due to equal M_6 and M_7 currents, the voltage applied at Y is conveyed to node X [9]. No external mirrors are necessary for the current at node X to be conveyed to node Z. Table 1 summarizes the aspect ratios of the CCII's MOS devices.

Table 1. CCII MOSFET Aspect Ratios

MOSFET	Aspect Ratio
$M_1 - M_4$	8.4µm/1.2µm

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$M_5 – M_8$	4.8µm/1.2µm
M_9 , M_{10} , M_{12}	9.6µm/1.2µm
M_{11}	8.4µm/1.2µm m=10

$M_4 – M_7$	9.3µm/1.2µm m=4
M_8, M_9, M_{13}	5µm/1.2µm m=2
M_{10}, M_{11}, M_{14}	7.8µm/1.2µm m=2

2.3. Folded Cascode Operational Trans-conductance Amplifier

The FC-OTA has been chosen for the VCCS because of its relatively large gain-bandwidth product, a wide output swing, high slew rate and power supply rejection ratio (PSRR) that makes it useful for low voltage operation. Figure 4 shows the FC-OTA circuit.

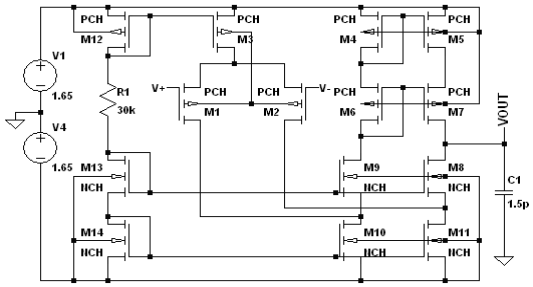

Figure 4. FC-OTA Circuit Schematic

The circuit is composed of a folded differential PMOS transistor pair M_1 and M_2. The folded architecture improves the DC gain of a typical differential pair with current source load and at the same time offers self compensation which is the drawback of single ended differential pairs. Use of PMOS transistors for the input stage offers a lower flicker noise as compared to NMOS. The transistors $M_4 – M_7$ form a cascode current mirror pair which offers a wider output swing as compared to the typical Wilson current source. The transistors $M_8 – M_{11}$ form a cascode current sink. The transistors M_8 and M_9 directly affect the stability of the FC-OTA. They define the second pole of the FC-OTA transfer function which sets its phase margin. The phase margin is the allowable input and output phase difference so that an amplifier does not oscillate or become unstable. A prescribed margin is 45deg. The capacitor C_1 sets the Gain-Bandwidth Product (GBP) of the FC-OTA and permits self compensation. Table 2 summarizes the aspect ratios of the FC-OTA's MOSFETs.

Table 2. FC-OTA MOSFET Aspect Ratio

MOSFET	Aspect Ratio
$M_1 – M_2$, M_3, M_{12}	7.4µm/1.2µm m=4

III. RESULTS AND DISCUSSION

This section presents the results of the HSPICE simulations of the different components of the proposed current source using the five process corners of the TSMC 0.35um 2P4M CMOS technology. These process corners consist of the Typical – Typical (TT), Fast – Fast (FF), Slow – Slow (SS), Slow – Fast (SF) and Fast – Slow (FS) cases. These corners represent the variations in the fabrication process that normally affects the charge mobility and therefore the speed of the MOS transistor. The overall circuitry is powered by a bipolar supply of +/- 1.65V.

3.1. CCII

The designed CCII has achieved a linear range from -0.77 to 0.181V with a slope of 0.964 and an offset voltage of 14.9mV in the X-terminal and 41.9mV in the Z-terminal. The voltage at the input Y-terminal has been successfully conveyed to the X-terminal with a 0.95 transfer factor (V_X/V_Y) over a bandwidth covering the beta dispersion range. Figure 5 shows the CCII's linear range while figure 6 shows the current ratio I_Z/I_X to elucidate the current conveying action of the CCII for the five process corners.

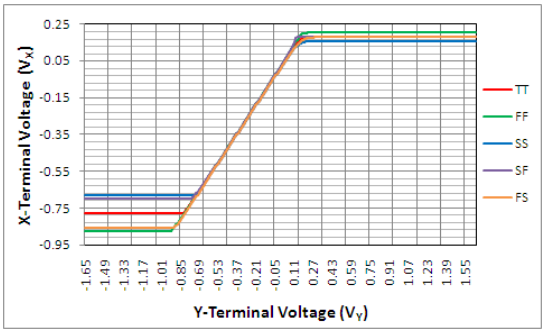

Figure 5. CCII's linear range

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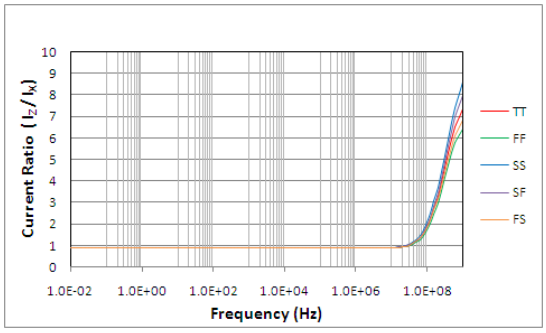

Figure 6. CCII's Z- and X-terminal current ratio (I_Z/I_X)

Based from figure 6, the CCII has an average current ratio of 0.84 that is constant up to 10MHz, with a standard deviation (σ) of just 0.047 for the five process corners. This confirms that the current drained in the X-terminal (I_X) is being conveyed or buffered to Z-terminal (I_Z). The output impedances of the CCII for the process corners are shown in figure 7.

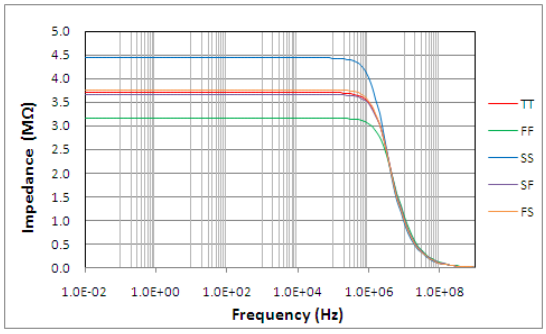

Figure 7. CCII's Output Impedance

It can be seen that the CCII has maintained an output impedance within 1MΩ even at the upper frequency of the beta dispersion range. This is essential so that the proposed current source will achieve high output impedance at such high frequency range. Its impedance is fairly constant up to 500 kHz. The CCII dissipates an average power of 350µW.

3.2. FC-OTA

Based from equation 1, the FC-OTA should have a high input and output impedance to contribute to the overall output impedance of the current source. The input and output impedance of the FC-OTA for the five process corners are shown in figures 8 and 9, respectively.

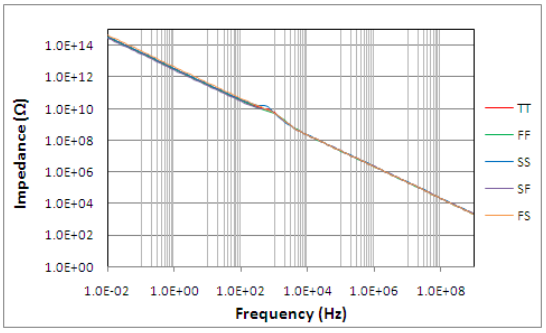

Figure 8. FC-OTA input impedance

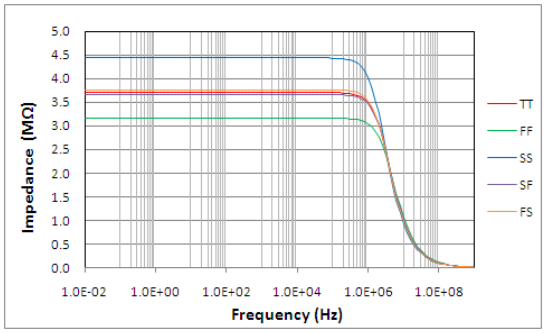

Figure 9. FC-OTA output impedance

The FC-OTA has achieved an input impedance from 220kΩ up to 225MΩ and an output impedance from 10.2kΩ up to 3.7MΩ within the beta dispersion range. Its input impedance is invariable with the process variations. Such values of impedances will help maintain relatively high output impedance throughout the target operating frequency range. Aside from the input and output impedances, the FC-OTA must also have high differential gain (A_D) and Common-Mode Rejection Ratio (CMRR) based from equation 1. The plots of the A_D and CMRR versus frequency for the five process corners are shown in figures 10 and 11, respectively.

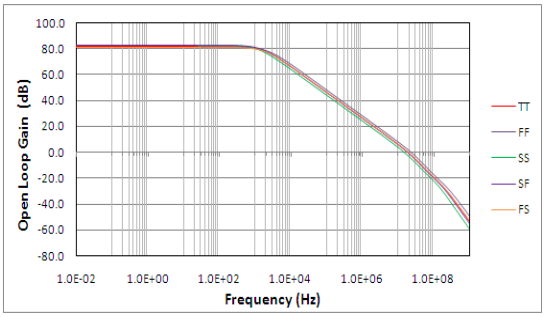

Figure 10. FC-OTA's Differential Open Loop Gain

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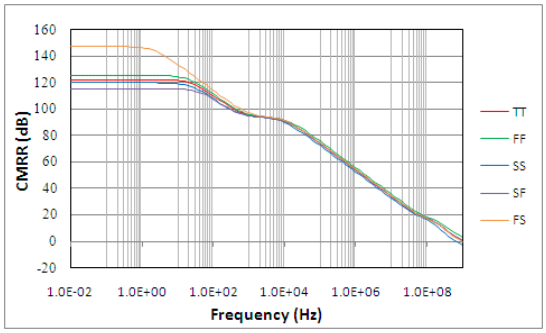

Figure 11. FC-OTA's CMRR

It can be seen, that the FC-OTA has a differential gain from 6dB to 66dB and a CMRR from 34dB to 91dB within the beta dispersion range. Along with the AC analysis done is the pole zero analysis which is a measure of both stability and linearity within the amplifier's transition frequency or UGBW. The resulting second pole of the FC-OTA's transfer function is located at 47MHz which is above the beta dispersion range. Such ensures that the output of the FC-OTA is linear within the operating bandwidth. Table 3 highlights the different performance specifications of the designed FC-OTA.

Table 3. FC-OTA performance specifications

	FABRICATION PROCESS CORNERS				
SPECIFICATION	TT	FF	SS	SF	FS
UGBW (Hz)	1.88E+07	2.33E+07	1.45E+07	1.80E+07	1.95E+07
DC Gain (dB)	8.06E+01	8.04E+01	8.03E+01	8.09E+01	8.02E+01
Phase Margin (deg)	7.04E+01	7.02E+01	7.11E+01	7.01E+01	7.08E+01
Z (in) @ 1MHz (Ω)	3.18E+06	3.19E+06	3.16E+06	3.21E+06	3.14E+06
Z (out) @1MHz (Ω)	1.02E+05	1.02E+05	1.02E+05	1.02E+05	1.02E+05

The FC-OTA has achieved an average UGBW of 18.8MHz, DC Open Loop Gain of 80.5dB, a Phase Margin of 70.5degrees, an input impedance and output impedance of 3.18MΩ and 102kΩ, respectively at 1MHz of frequency. The achieved phase margin ensures that the FC-OTA will not go into sustained oscillation or become unstable. The FC-OTA dissipates an average of 265µW

3.3. Inverting Amplifier Current Source

The FC-OTA has been configured as an inverting amplifier to function as a current source. This is shown in figure 12.

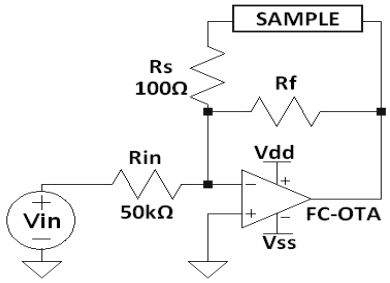

Figure12. Inverting amplifier current source

Its resulting output impedance for various feedback resistor (R_f) values are shown in figure 13. Note that the series resistor (R_S) at the feedback loop is set to 100Ω to serve as an over-current protection to the biological sample and the resistor at the inverting input (R_{in}) is 50kΩ.

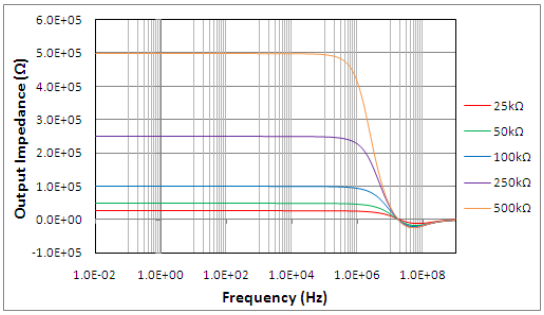

Figure 13. FC-OTA – based current source output impedance for various feedback resistor values

It can be seen that the resulting output impedance is a strong function of R_f. A closer look at the roll off at the high frequency end shows the increasing error percentage with frequency. This is shown in figure 14.

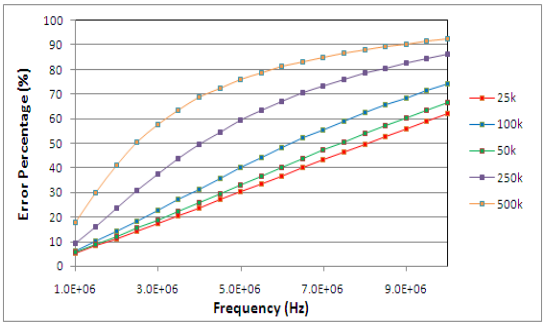

Figure 14. Output impedance error percentage in the 1MHz to 10MHz bandwidth

The error percentage tells the extent of roll-off in the upper range of the beta dispersion. This is obtained by taking the difference of the resulting

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output impedance to the value of R_f since the latter serves as the low frequency impedance. Such large roll-off with frequency will affect the current distribution to the sample and would cause inaccuracy in the excitation level and hence errors in the resolution of bio-impedance.

3.4. Designed Current Source

Referring back to figure 1, the designed current source is composed of a Norton current source driving Voltage Controlled Current Source (VCCS). The Norton current source is realized using a CCII. This approach tends to improve the output impedance of a typical VCCS especially at high operating frequencies. Figure 15 shows the output impedance of the current source for various R_f values with $R_x = R_z = 50k\Omega$.

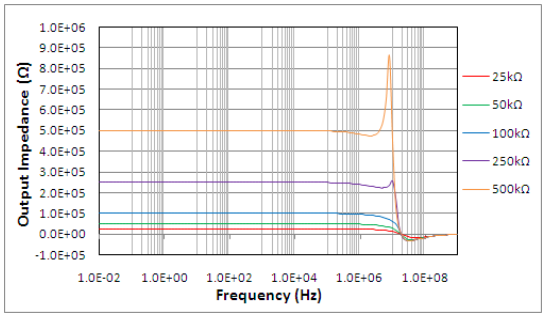

Figure 15. Output impedance of the designed current source for various R_f values

It can be seen that the output impedance of the current source resembles that of the R_f. This means that the equivalent impedance to which R_f is effectively in parallel, as shown in equation 1, is very large as compared to it. Hence by virtue of parallel resistors, R_f influences the output impedance more. The output impedance of the current source may therefore be increased linearly by varying R_f.

The corresponding output impedances for the five process corners are shown in figure 16. These graphs were obtained using an R_f of 50kΩ.

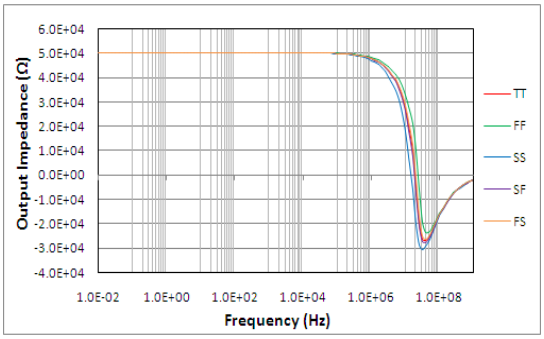

Figure 16. Output impedance of the designed current with $R_f = 50k\Omega$ for the five process corners

It can be seen that process variations have no significant effect on the output impedance. An average impedance of 48kΩ with a standard deviation of 1.05kΩ is obtained at 1MHz for the five process corners. A comparison of the output impedances of the VCCS and the designed current source are shown in figures 17 and 18 for the 1MHz to 10MHz band.

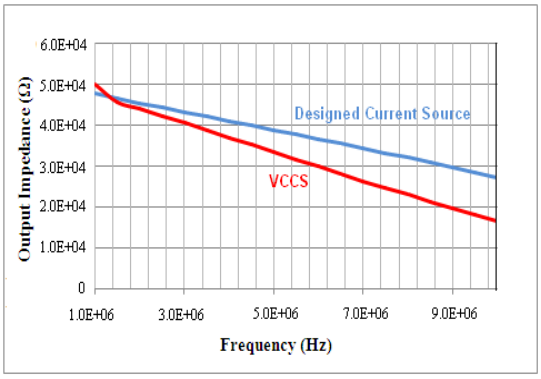

Figure 17. Comparison of the output impedances of both current sources for $R_f = 50k\Omega$

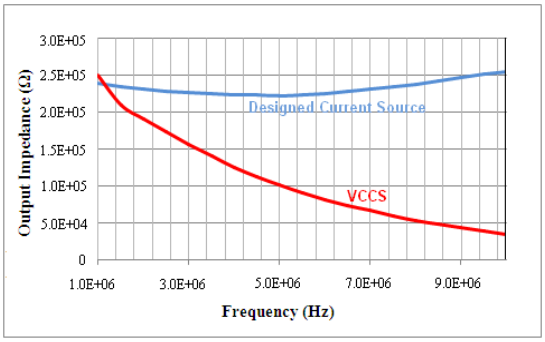

Figure 18. Comparison of the output impedances of both current sources for $R_f = 250k\Omega$

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It can be seen that the designed current source has achieved higher output impedance as compared to the VCCS for the 1MHz to 10MHz band. The improvement in the output impedance lessens the potential loading effect that the parasitic impedance of the current source can cause onto the sample.

The effect of various loads on the magnitude of the excitation current has also been verified. Loads of 100Ω, 250Ω, 500Ω, 1kΩ, 2.5kΩ, 5kΩ and 10kΩ were used. For the transient simulation, the peak-peak current was obtained for each load and process corner. The overall standard deviation of the output current level under various loads lies within 0.18μA having an average current level of 3.20μA. For a fixed load under various process corners, the standard deviation is just 100nA. These data are obtained by using an input drive voltage of 0.1V and 10MHz of frequency. Such input amplitude serves as the maximum input drive voltage to keep the MOSFETs in saturation and avoid distortion. HSPICE simulations show that this is the maximum input amplitude to produce an undistorted output current signal at 10MHz of frequency.

The quality of the output current signal under different loads and process corners has also been verified using the frequency domain analysis. A 1024-point FFT using a rectangular window was done to yield the characteristics of the signal such as Total Harmonic Distortion (THD), Signal-Noise Ratio (SNR) and Spurious Free Dynamic Range (SFDR) Figures 19 and 20 show the output current signal in time and frequency domains respectively for a 100Ω load.

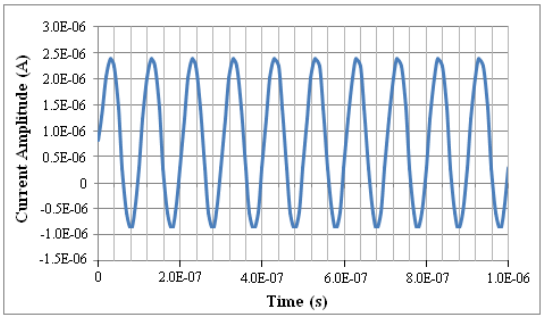

Figure 19. Current source output signal in time domain

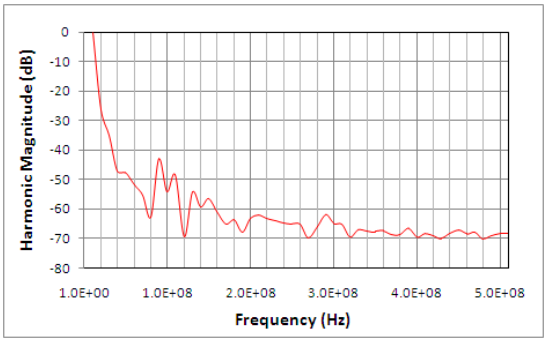

Figure 20. Current source output signal FFT spectrum

The results of the FFT analysis are summarized in Table 4. The analysis considers the first 30 harmonics of the 10MHz fundamental frequency in its computation of THD, SNR and SFDR.

Table 4. FFT analysis results

FFT Parameters	Process Corners				
	TT	FF	SS	SF	FS
THD (dB)	-25.99	-27.35	-23.94	-24.60	-26.57
SNR (dB)	34.14	35.47	32.55	33.55	34.19
SFDR (dB)	26.75	28.22	24.37	25.33	27.11

The excitation current signal has an average THD, SNR and SFDR of -25.69dB, 33.98dB, and 26.36dB respectively. The resulting THD ensures that the current signal delivered to the load is almost a pure signal avoiding higher ordered dispersions. The SNR and SFDR are also sufficient for a low amplitude and high frequency signal. This is also significant for circuits operating in low power. The corresponding standard deviations of the THD, SNR and SFDR for sample loads from 100Ω to 5kΩ are 0.104dB, 0.172dB, and 0.094dB respectively. Hence, the amount of load has no significant effect on the quality of the excitation current signal. The linear operating range of the designed current source was verified under different sample loads as shown in figure 21.

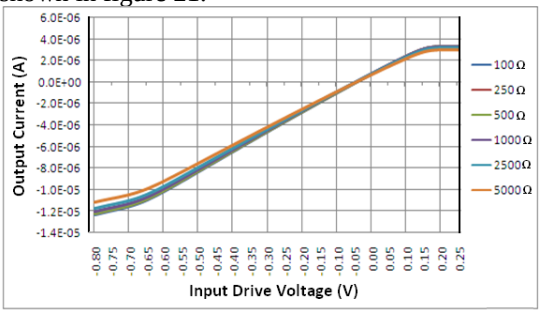

Figure 21. Designed current source linear range for various loads

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The current source has achieved a linear range from -0.80V to 0.15V with regard to the input voltage level. It has a voltage-current conversion factor or sensitivity of 0.154µA/V with an offset of -12.1µA. A standard deviation of 12.31nA/V in the sensitivity was obtained for the five process corners. This signifies that the output current is fairly constant under process variations.The designed current source dissipates an average power of 600µW for a bipolar supply of +/- 1.65 V regardless of the value of the feedback resistor. The circuit however may still be operated at +/- 1.6V to dissipate an average of 543µW without altering the strong inversion conditions of the MOSFETs.

IV. CONCLUSION

A high output impedance current source for use in wideband BI applications has been designed and presented. It is based from TSMC 0.35µm CMOS 2P4M technology composed of a CCII driving a VCCS. The CCII acts as a Norton current source that has successfully increased the output impedance especially on the high frequency end of the beta dispersion range. The output impedance of the designed current source can be configured with a relatively high degree of accuracy by just setting the feedback resistor of the VCCS. This has been possible due to the high output impedance of the CCII, the high input and output impedances, A_D, and CMRR of the FC-OTA even up to 10MHz. The current source has a sensitivity of about 0.154µA/V and a linear range from -0.80V to 0.15V of input voltage. Load variations have no significant effect on the current source's linear range, operating frequency and signal integrity as shown by the FFT analysis results. The circuit dissipates an average of 600µW. The design can provide a distortion-less current signal of about 3.2µA which is sufficient for cellular suspension BI applications. This can further be improved with the use of rail-rail type of CCII and FC-OTA that will effectively increase the linear range.

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